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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/007,498	11/13/2001	Hung T. Nguyen	01-625	2278

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EXAMINER	
MEONSKE, TONIA L	
ART UNIT	**PAPER NUMBER**
2181	

DATE MAILED: 06/20/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/007,498	NGUYEN ET AL.	
	Examiner	Art Unit	
	Tonia L. Meonske	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 April 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5,7-12 and 14-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5, 7-12 and 14-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

FRITZ FLEMING
SUPERVISORY PRIMARY EXAMINER
GROUP 2100
6/12/2006

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on April 4, 2006 has been entered.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-5 and 7-14 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by DeGroot, US Patent 4,683,547, cited by Examiner on August 18, 2005 (herein referred to as DeGroot).

4. Referring to claim 1, DeGroot has taught for use in a processor having an at least four-wide instruction issue architecture, a mechanism for pipeline processing multiply-accumulate instructions with out-of-order completion, comprising:

a. instruction grouping logic implementing instruction grouping rules (abstract, Figure 1, column 2, lines 25-40, column 3, line 3-column 4, line 33, Column 5, line 9-column 8, line 6, Multiply and accumulate instructions are grouped to execute simultaneously such that a result is produced by both the ADD and Multiply units each

cycle. One rule is that a maximum of two instructions may be grouped to produce results each cycle. Another rule is that only ready instructions are grouped to execute together.);

b. a multiply-accumulate unit (MAC) having an initial multiply stage and a subsequent accumulate stage (abstract, Figure 1, column 2, lines 25-40, column 3, line 3-column 4, line 33); and

c. out-of-order completion logic, associated with said MAC, that causes interim results produced by said multiply stage to be stored when said accumulate stage is unavailable and allows younger instructions to complete before said multiply-accumulate instructions (Figures 1 and 3, column 5, line 19-column 6, line 41), said multiply-accumulate instructions being grouped based on said rules (Column 5, lines 65-column 6, line 5, abstract, Figure 1, column 2, lines 25-40, column 3, line 3-column 4, line 33, Column 5, line 9-column 8, line 6, Instructions in both pipelines that are ready to execute are grouped to execute simultaneously. Multiply and accumulate instructions are grouped to execute simultaneously such that a result is produced by both the ADD and Multiply units each cycle. One rule is that a maximum of two instructions may be grouped to produce results each cycle. Another rule is that only ready instructions are grouped to execute together.).

5. Referring to claim 2, DeGroot has taught the mechanism as recited in Claim 1, as described above, and wherein said initial multiply stage and said subsequent accumulate stage are single clock cycle stages (column 7, lines 52-61, column 8, lines 20-25, column 3, lines 38-43).

6. Referring to claim 3, DeGroot has taught the mechanism as recited in Claim 1, as described above, and wherein said out-of-order completion logic is contained in a writeback stage of a pipeline in said processor (Figures 1 and 3, column 5, line 19-column 6, line 41).

7. Referring to claim 4, DeGroot has taught the mechanism as recited in Claim 1, as described above, and wherein said out-of-order completion logic writes back said interim results to at least one register in said MAC before said multiply-accumulate instructions arrive at said accumulation stage of said MAC (Figures 1 and 3, column 5, line 19-column 6, line 41, Interim results are written to the wait stations and element 8 before the results arrive at element 2.).

8. Referring to claim 5, DeGroot has taught the mechanism as recited in Claim 1, as described above, and wherein said interim results are unavailable to an external program executing in said processor (abstract, Figure 1, column 2, lines 25-40, column 3, line 3-column 4, line 33, Interim results are unavailable to the original external FORTRAN code. The interim results are specifically for the optimized transformed code.).

9. Referring to claim 7, DeGroot has taught the mechanism as recited in Claim 1, as described above, and wherein said processor is a digital signal processor (abstract, Figures 1 and 3, The processor processes digital signals, therefore the processor is a digital signal processor.).

10. Claims 8-12 and 14 do not recite limitations above the claimed invention set forth in claims 1-5 and 7 and are therefore rejected for the same reasons set forth in the rejection of claims 1-5 and 7 above.

Claim Rejections - 35 USC § 103

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

12. Claims 15-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over DeGroot, US Patent 4,683,547, cited by Examiner on August 18, 2005 (herein referred to as DeGroot) in view of Chamdani et al., US Patent 6,112,019, cited by Examiner on August 18, 2005 (herein referred to as Chamdani).

13. Referring to claim 15, DeGroot has taught a digital signal processor (DSP), comprising:

A. a pipeline having stages and capable of processing multiply-accumulate instructions (column 3, line 3-column 4, line 33);

b. an instruction issue unit containing grouping logic implementing instruction grouping rules (Column 5, lines 65-column 6, line 5, abstract, Figure 1, column 2, lines 25-40, column 3, line 3-column 4, line 33, Column 5, line 9-column 8, line 6, Instructions in both pipelines that are ready to execute are grouped to execute simultaneously. Multiply and accumulate instructions are grouped to execute simultaneously such that a result is produced by both the ADD and Multiply units each cycle. One rule is that a maximum of two instructions may be grouped to produce results each cycle. Another rule is that only ready instructions are grouped to execute together.);

c. a multiply-accumulate unit (MAC), coupled to said instruction issue logic, having an initial multiply stage and a subsequent accumulate stage (abstract, Figure 1, column 2, lines 25-40, column 3, line 3-column 4, line 33); and

d. out-of-order completion logic, associated with said pipeline, that causes interim results produced by said multiply stage to be stored when said accumulate stage is

unavailable and allows younger instructions to complete before said multiply-accumulate instructions (Figures 1 and 3, column 5, line 19-column 6, line 41), said multiply-accumulate instructions being grouped according to said rules (Column 5, lines 65-column 6, line 5, abstract, Figure 1, column 2, lines 25-40, column 3, line 3-column 4, line 33, Column 5, line 9-column 8, line 6, Instructions in both pipelines that are ready to execute are grouped to execute simultaneously. Multiply and accumulate instructions are grouped to execute simultaneously such that a result is produced by both the ADD and Multiply units each cycle. One rule is that a maximum of two instructions may be grouped to produce results each cycle. Another rule is that only ready instructions are grouped to execute together.).

14. DeGroot has not specifically taught at least four-wide instruction issue logic. However, issuing multiple instructions is well known in the art in order to achieve parallel execution within a processor. One such teaching of this fact is described in Chamdani at column 2, lines 10-14. Furthermore, it has been held that a change in size is not a patentable difference. See *In re Rose*, 220 F.2d 459, 463, 105 USPQ 237, 240 (CCPA 1955). So issuing any number of instructions, including four, would have been obvious to one of ordinary skill in the art at the time the invention was made. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have the invention of DeGoot, include a four-wide instruction issue logic, as taught by Chamdani and *In re Rose,* for the desirable purpose of achieving parallel execution within a processor.

15. Claims 16-19 do not recite limitations above the claimed invention set forth in claims 2-5 and are therefore rejected for the same reasons set forth in the rejection of claims 2-5 above.

Response to Arguments

16. Applicant's arguments filed April 4, 2006 have been fully considered but they are not persuasive.

17. On pages 6, Applicant argues with respect to claim 1 and similarly with respect to claim 8 in essence:

> *"Claim 1 includes the elements "instruction grouping logic implementing instruction grouping rules" and "multiply-accumulate instructions being grouped based on said rules." DeGroot does not teach these elements, and therefore does not anticipate Claim 1."*

However, DeGroot has taught *"instruction grouping logic implementing instruction grouping rules" and "multiply-accumulate instructions being grouped based on said rules."* (abstract, Figure 1, column 2, lines 25-40, column 3, line 3-column 4, line 33, Column 5, line 9-column 8, line 6) In DeGroot multiply and accumulate instructions are grouped to execute simultaneously such that a result is produced by both the ADD and Multiply units each cycle. One rule is that a maximum of two instructions may be grouped to produce results each cycle. Another rule is that only ready instructions are grouped to execute together. So DeGroot has in fact taught *"instruction grouping logic implementing instruction grouping rules" and "multiply-accumulate instructions being grouped based on said rules."* (abstract, Figure 1, column 2, lines 25-40, column 3, line 3-column 4, line 33, Column 5, line 9-column 8, line 6) Also see the rejection of claim1 above. Therefore this argument is moot.

18. On page 7, Applicant argues in essence:

> *"Claims 15-19 include the elements "an instruction issue unit, containing grouping logic implementing instruction grouping rules," and "multiply-accumulate instructions being*

grouped based on said rules." The examiner does not cite the references for teaching these elements, and Applicants do not find such a teaching therein."

However, DeGroot has taught *"an instruction issue unit, containing grouping logic implementing instruction grouping rules," and "multiply-accumulate instructions being grouped based on said rules."* (Column 5, lines 65-column 6, line 5, abstract, Figure 1, column 2, lines 25-40, column 3, line 3-column 4, line 33, Column 5, line 9-column 8, line 6) In DeGroot instructions in both pipelines that are ready to execute are grouped to execute simultaneously. Multiply and accumulate instructions are grouped to execute simultaneously such that a result is produced by both the ADD and Multiply units each cycle. One rule is that a maximum of two instructions may be grouped to produce results each cycle. Another rule is that only ready instructions are grouped to execute together. So DeGroot has in fact taught *"an instruction issue unit, containing grouping logic implementing instruction grouping rules," and "multiply-accumulate instructions being grouped based on said rules."* (Column 5, lines 65-column 6, line 5, abstract, Figure 1, column 2, lines 25-40, column 3, line 3-column 4, line 33, Column 5, line 9-column 8, line 6) Also see the rejection of claim 15 above. Therefore this argument is moot.

Conclusion

19. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tonia L. Meonske whose telephone number is (571) 272-4170. The examiner can normally be reached on Monday-Friday, with every other Friday off.

20. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Fritz Fleming can be reached on (571) 272-4145. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

21. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

tlm

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